IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Theodore W. Houston	Docket No.: TI-32205.1
Serial No.: 10/664,547	Art Unit: 2894
Filed: 09/19/2003	Examiner: Lewis, Monica

Confirmation No. 4290

Title: Integrated DRAM Process/Structure Using Contact Pillars

APPELLANT'S BRIEF

December 28, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the final Office Action, dated 08/20/2008, and the Notice of Appeal, dated 12/28/2008, the Appellant submits this Brief. The Commissioner is hereby requested and authorized to charge any required fees for the filing of this document to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

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REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Texas Instruments Incorporated, the assignee, as evidenced by the assignment carried from the original application and set forth at Reel 013059, Frame 0497.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to the Appellant.

STATUS OF CLAIMS

Claims 49-54 are the subject of this appeal. Claims 49-54 are pending and rejected. Claims 1-48 and 55-56 are cancelled.

STATUS OF AMENDMENTS

The Appellant filed a Preliminary Amendment dated September 19, 2003. The Appellant filed an amendment, dated July 25, 2005, in response to the non-final Office Action dated February 25, 2005. The Appellant filed an amendment, dated January 9, 2006, in response to the non-final Office Action dated October 20, 2005. The Appellant filed a Request to Withdraw the Notice of Abandonment and an amendment, dated October 26, 2006, in response to the Notice of Abandonment dated October 6, 2006 and the final Office Action dated March 27, 2006. The Appellant filed a Request for Continued Examination dated August 28, 2007. The Appellant filed a Supplemental Request to Withdraw the Notice of Abandonment, dated September 24, 2007. The Petition was granted September 27, 2007. The Appellant filed a supplemental amendment, dated November 29, 2007, in response to voice messages received from the Examiner on November 21, 2007 and November 29, 2007.

The Appellant filed an amendment, dated May 19, 2008, in response to the non-final Office Action dated February 26, 2008. The Appellant files this Appellant's Brief in response to the final Office Action dated August 20, 2008.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 49 is directed to an integrated circuit (page 6 lines 11-14; page 7 lines 1-10; page 21 line 24 through page 23 line 22; element 1305 of FIG. 22 and element 1350 of FIG. 23). A first insulating layer (page 22 lines 14-16 and 26-27, page 23 lines 8-11 and 18; element 265 of FIG. 23) is disposed between a substrate (page 22 line 17; element 202 of FIG. 23) and a first metal layer (page 23 lines 1-5 and 20-22; elements 218, 1375, and 280 of FIGS. 22-23). A trench (page 22 lines 7-9, 16-20 and 26-27; page 23 lines 5-14; element 1310 of FIG. 22) is defined by a recess in the first insulating layer (page 22 lines 13-19), the trench not extending below a top surface of the substrate (page 22 lines 16-19; page 23 lines 8-11; FIG. 23). A first contact pillar (page 22 lines 4-5, 20-21 and 30; page 23 lines 1 and 11-12; element 225 of FIGS. 22-23) extends substantially from the top surface of the substrate to a bottom surface of the first metal layer within the trench (page 22 lines 19-21; FIG. 23). A capacitor (page 22 lines 19-30; page 23 lines 1, and 8-16; elements 1366, 225, 1367, 1368 and 1375 of FIGS. 22 and 23) is formed in the trench overlying the first contact pillar such that the capacitor is formed (page 22 lines 19-21; page 23 lines 11-14; FIG. 23) at least in part on a side of the first contact pillar (page 22 lines 19-21; page 23 lines 11-14; FIG. 23), and the first contact pillar is a first plate (page 22 lines 7-9, 19-21; page 23 lines 11-14; FIG. 23) of the capacitor.

Claim 50 is dependent on Claim 49 and further specifies a second contact pillar (page 23 lines 1-5 and 19-22; element 230 of FIGS. 22 and 23) extending substantially from the top surface of the substrate to a bottom surface of another portion of the first metal layer (FIG. 23), wherein the second contact pillar is substantially the same height as the first contact pillar (page 23 lines 1-5 and 19-22; element 230 of FIGS. 22 and 23).

Claim 51 is dependent on Claim 49 and further specifies that the capacitor comprises a storage element of a memory cell (page 4 line 29 through page 5 line 17; page 10 line 21 through page 11 line 18; page 12 lines 9-10; page 22 lines 10-11).

Claim 52 is dependent on Claim 51 and further specifies that a storage node of the storage element comprises the first contact pillar (page 22 lines 5-9; element 214 of FIGS. 22 and 23).

Claim 53 is dependent on Claim 52 and further specifies that the storage node further comprises a conducting layer lining the trench and the side of the first contact pillar (page 22 lines 7-9; page 23 lines 11-14; FIG. 23).

Claim 54 is dependent on Claim 50 and further specifies that the second contact pillar is a bit line contact pillar (page 23 lines 1-5 and 19-22; element 230 of FIGS. 22 and 23).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 49-52 and 54 stand rejected under 35 U.S.C. §103(a) as unpatentable over the patent granted to Turner (U.S. Pat. No. 5,357,132) in view of Kurosawa et al. (U.S. Pat. No. 4,951,175).

2. Claim 53 stands rejected under 35 U.S.C. §103(a) as unpatentable over the patent granted to Turner (U.S. Pat. No. 5,357,132) in view of Kurosawa et al. (U.S. Pat. No. 4,951,175) and Fisher et al. (U.S. Pat. No. 5,962,885).

ARGUMENT

Rejection of Claims 49-52 and 54 under 35 U.S.C. §103(a) as unpatentable over the patent granted to Turner (U.S. Pat. No. 5,357,132) in view of Kurosawa et al. (U.S. Pat. No. 4,951,175).

Claim 49

Independent Claim 49 positively recites a first contact pillar extending substantially from the top surface of the substrate to a bottom surface of the first metal layer within the trench. These advantageously claimed features are not taught or suggested by the patents granted to Turner or Kurosawa et al.; either alone or in combination.

Turner does not teach the advantageously claimed invention because Turner does not teach a first contact pillar extending substantially to a bottom surface of the first metal layer within the trench (column 5 lines 59-62; column 6 lines 16-19; FIGS. 10-12). Similarly, Kurosawa et al. does not teach the advantageously claimed invention because Kurosawa et al. does not teach a first contact pillar extending substantially to a bottom surface of the first metal layer within the trench (column 3 lines 56-63; FIGS. 2 and 5G). Therefore, the combination of Turner and Kurosawa et al. also does not teach a first contact

pillar extending substantially to a bottom surface of the first metal layer within the trench, as advantageously claimed.

The Appellant respectfully traverses the statement in the Office Action (page 2) that Turner teaches "a first contact pillar (64) extending substantially...to a bottom surface of the first metal layer (68)." The Appellant submits that the first metal layer of Turner cannot be element 68 because element 68 of Turner is part of the capacitor (column 5 lines 44-54) and the capacitor is a separately claimed element from the first metal layer in the Appellant's Claim 49.

The Appellant also respectfully traverses the statement in the Office Action (pages 2-3) that it "would have been obvious to one having ordinary skill in the art at the time of the invention was made" to combine teachings of Turner with teachings of Kurosawa et al. The Appellant submits that trench capacitors and stacked capacitors are separate (alternative) capacitor constructions (see Turner column 1 lines 41-48 or Appellant's Specification page 3 line 13). The Appellant also submits that Turner teaches that "the only technique that has been utilized with any success in high density DRAMs is the trench capacitor cell" (column 1 lines 49-51). Therefore, Turner teaches away from being combined with Kurosawa et al.'s teaching of "the present invention is addressed to a specific semiconductor memory device which has a memory cell with a stacked capacitor cell" (column 2 lines 8-16).

Furthermore, the Appellant submits that one having ordinary skill in the art at the time of the invention would not modify Turner to include the trench disclosed in Kurosawa et al. because the trench (element 48) taught by Turner is an isolation trench (column 4 lines 56-58; FIG. 7) and the trench of Kurosawa et al. (FIG. 2; column 2 lines 17-21) cannot be an isolation trench (because that would leave the diffusion layer 14 operational – compared to the trench of Turner that renders the diffusion layer 44 inoperable).

Therefore, Claim 49 is patentable over Turner and Kurosawa et al.

Claim 50

Claim 50 is dependent on Claim 49 and is therefore allowable for the same reasons that Claim 49 is allowable. Furthermore, Claim 50 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 49, are not taught nor suggested by the patents granted to Turner or Kurosawa et al.; either alone or in combination. Namely, Claim 50 further specifies the additional limitation that a second contact pillar extends substantially from the top surface of the substrate to a bottom surface of another portion of the first metal layer, wherein the second contact pillar is substantially the same height as the first contact pillar.

Turner does not teach the advantageously claimed invention because Turner does not teach a second contact pillar extending substantially to a bottom surface of the first metal layer within the trench (column 5 lines 59-62; column 6 lines 16-19; FIGS. 10-12). Similarly, Kurosawa et al. does not teach the advantageously claimed invention because Kurosawa et al. does not teach a second contact pillar extending substantially to a bottom surface of the first metal layer within the trench (column 3 lines 56-63; FIGS. 2 and 5G). Therefore, the combination of Turner and Kurosawa et al. also does not teach a second contact pillar extending substantially to a bottom surface of the first metal layer within the trench, as advantageously claimed.

The Appellant respectfully traverses the statement in the Office Action (page 3) that Turner teaches "a second contact pillar (62) extending substantially...to a bottom surface of the first metal layer... (For example: See Figure 9)." The Appellant submits that FIG. 9 of Turner does not show the first metal layer; therefore FIG. 9 of Turner does not teach "a second contact pillar (62) extending substantially...to a bottom surface of the first metal layer".

The Appellant also respectfully traverses the statement in the Office Action (pages 2-3) that it "would have been obvious to one having ordinary skill in the art at the time of the invention was made" to combine teachings of Turner

with teachings of Kurosawa et al. The Appellant submits that trench capacitors and stacked capacitors are separate (alternative) capacitor constructions (see Turner column 1 lines 41-48 or Appellant's Specification page 3 line 13). The Appellant also submits that Turner teaches "the only technique that has been utilized with any success in high density DRAMs is the trench capacitor cell" (column 1 lines 49-51). Therefore, Turner teaches away from being combined with Kurosawa et al.'s teaching of "the present invention is addressed to a specific semiconductor memory device which has a memory cell with a stacked capacitor cell" (column 2 lines 8-16).

Therefore, Claim 50 is patentable over Turner and Kurosawa et al.

Claim 51

Claim 51 is dependent on Claim 49 and is therefore allowable for the same reasons that Claim 49 is allowable. Furthermore, Claim 51 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claim 49, are not taught nor suggested by the patents granted to Turner or Kurosawa et al.; either alone or in combination. Namely, the combination of Claims 49 and 51 further specifies that the capacitor is formed in the trench overlying the first contact pillar that extends substantially to the first metal layer and the capacitor comprises a storage element of a memory cell.

Turner does not teach the advantageously claimed invention because Turner does not teach a capacitor that is formed in the trench overlying a first contact pillar extending substantially to a bottom surface of the first metal layer (column 5 lines 59-62; column 6 lines 16-19; FIGS. 10-12). Similarly, Kurosawa et al. does not teach the advantageously claimed invention because Kurosawa et al. does not teach a capacitor that is formed in the trench overlying a first contact pillar extending substantially to a bottom surface of the first metal layer (column 3 lines 56-63; FIGS. 2 and 5G). Therefore, the combination of Turner and Kurosawa et al. also does not teach a capacitor that is formed in the trench overlying a first contact pillar extending substantially to a bottom surface of the first metal layer, as advantageously claimed.

The Appellant respectfully traverses the statement in the Office Action (pages 2-3) that it "would have been obvious to one having ordinary skill in the art at the time of the invention was made" to combine teachings of Turner with teachings of Kurosawa et al. The Appellant submits that trench capacitors and stacked capacitors are separate (alternative) capacitor constructions (see Turner column 1 lines 41-48 or Appellant's Specification page 3 line 13). The Appellant also submits that Turner teaches "the only technique that has been utilized with any success in high density DRAMs is the trench capacitor cell" (column 1 lines 49-51). Therefore, Turner teaches away from being combined with Kurosawa et

al.'s teaching of "the present invention is addressed to a specific semiconductor memory device which has a memory cell with a stacked capacitor cell" (column 2 lines 8-16).

Therefore, Claim 51 is patentable over Turner and Kurosawa et al.

Claim 52

Claim 52 is dependent on Claims 49 and 51 and is therefore allowable for the same reasons that Claims 49 and 51 are allowable. Furthermore, Claim 52 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 49 and 51, are not taught nor suggested by the patents granted to Turner or Kurosawa et al.; either alone or in combination. Namely, the combination of Claims 49, 51, and 52 further specifies that a storage node comprises the first contact pillar that extends substantially to the first metal layer.

Turner does not teach the advantageously claimed invention because Turner does not teach a storage node that comprises the first contact pillar extending substantially to a bottom surface of the first metal layer (column 5 lines 59-62; column 6 lines 16-19; FIGS. 10-12). Similarly, Kurosawa et al. does not teach the advantageously claimed invention because Kurosawa et al. does not

teach a storage node that comprises the first contact pillar extending substantially to a bottom surface of the first metal layer (column 3 lines 56-63; FIGS. 2 and 5G). Therefore, the combination of Turner and Kurosawa et al. also does not teach a storage node that comprises the first contact pillar extending substantially to a bottom surface of the first metal layer, as advantageously claimed.

The Appellant respectfully traverses the statement in the Office Action (pages 2-3) that it "would have been obvious to one having ordinary skill in the art at the time of the invention was made" to combine teachings of Turner with teachings of Kurosawa et al. The Appellant submits that trench capacitors and stacked capacitors are separate (alternative) capacitor constructions (see Turner column 1 lines 41-48 or Appellant's Specification page 3 line 13). The Appellant also submits that Turner teaches "the only technique that has been utilized with any success in high density DRAMs is the trench capacitor cell" (column 1 lines 49-51). Therefore, Turner teaches away from being combined with Kurosawa et al.'s teaching of "the present invention is addressed to a specific semiconductor memory device which has a memory cell with a stacked capacitor cell" (column 2 lines 8-16).

Therefore, Claim 52 is patentable over Turner and Kurosawa et al.

Claim 54

Claim 54 is dependent on Claims 49 and 50, and is therefore allowable for the same reasons that Claims 49 and 50 are allowable. Furthermore, Claim 54 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 49 and 50, are not taught nor suggested by the patents granted to Turner or Kurosawa et al.; either alone or in combination. Namely, Claim 54 further specifies the additional limitation that a bit line contact pillar extends substantially from the top surface of the substrate to a bottom surface of another portion of the first metal layer, wherein the bit line contact pillar is substantially the same height as the first contact pillar.

Turner does not teach the advantageously claimed invention because Turner does not teach a bit line contact pillar that is substantially the same height as the first contact pillar (column 5 lines 55-68; FIGS. 10-12). Similarly, Kurosawa et al. does not teach the advantageously claimed invention because Kurosawa et al. does not teach a bit line contact pillar that is substantially the same height as the first contact pillar (column 3 lines 56-63; FIGS. 2 and 5G). Therefore, the combination of Turner and Kurosawa et al. also does not teach a bit line contact pillar that is substantially the same height as the first contact pillar, as advantageously claimed.

The Appellant respectfully traverses the statement in the Office Action (pages 2-3) that it "would have been obvious to one having ordinary skill in the art at the time of the invention was made" to combine teachings of Turner with teachings of Kurosawa et al. The Appellant submits that trench capacitors and stacked capacitors are separate (alternative) capacitor constructions (see Turner column 1 lines 41-48 or Appellant's Specification page 3 line 13). The Appellant also submits that Turner teaches "the only technique that has been utilized with any success in high density DRAMs is the trench capacitor cell" (column 1 lines 49-51). Therefore, Turner teaches away from being combined with Kurosawa et al.'s teaching of "the present invention is addressed to a specific semiconductor memory device which has a memory cell with a stacked capacitor cell" (column 2 lines 8-16).

Therefore, Claim 54 is patentable over Turner and Kurosawa et al.

Rejection of Claim 53 under 35 U.S.C. §103(a) as unpatentable over the patent granted to Turner (U.S. Pat. No. 5,357,132) in view of Kurosawa et al. (U.S. Pat. No. 4,951,175) and Fisher et al. (U.S. Pat. No. 5,962,885).

Claim 53

Claim 53 is dependent on Claims 49, 51, and 52, and is therefore allowable for the same reasons that Claims 49, 51, and 52 are allowable. Furthermore, Claim 53 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitations of Claims 49, 51, and 52, are not taught nor suggested by the patents granted to Turner, Kurosawa et al., or Fisher et al.; either alone or in combination. Namely, the combination of Claims 49, 51, 52, and 53 further specifies a conducting layer lining the side of the first contact pillar where the first contact pillar extends substantially to a bottom surface of the first metal layer within the trench.

Fisher et al. does not teach the advantageously claimed invention because Fisher et al. does not teach a conducting layer lining the side of the first contact pillar that extends substantially to a bottom surface of the first metal layer within the trench (column 3 lines 33-35; FIGS. 3, 5-7 and 9-10). In addition, Turner does not teach the advantageously claimed invention because Turner does not teach a conducting layer lining the side of the first contact pillar that

extends substantially to a bottom surface of the first metal layer within the trench (column 5 lines 59-62; column 6 lines 16-19; FIGS. 10-12). Similarly, Kurosawa et al. does not teach the advantageously claimed invention because Kurosawa et al. does not teach a conducting layer lining the side of the first contact pillar that extends substantially to a bottom surface of the first metal layer within the trench (column 3 lines 56-63; FIGS. 2 and 5G). Therefore, the combination of Fisher et al., Turner, and Kurosawa et al. also does not teach a conducting layer lining the side of the first contact pillar where the first contact pillar extends substantially to a bottom surface of the first metal layer within the trench, as advantageously claimed.

The Appellant respectfully traverses the statement in the Office Action (page 4) that it "would have been obvious to one having ordinary skill in the art at the time of the invention was made" to combine teachings of Turner with teachings of Kurosawa et al. and Fisher et al. The Appellant submits that trench capacitors and stacked capacitors are separate (alternative) capacitor constructions (see Fisher et al. column 1 lines 23-25, Turner column 1 lines 41-48, or Appellant's Specification page 3 line 13). The Appellant also submits that Turner teaches "the only technique that has been utilized with any success in high density DRAMs is the trench capacitor cell" (column 1 lines 49-51). Therefore, Turner teaches away from being combined with Kurosawa et al.'s teaching of "the present invention is addressed to a specific semiconductor

memory device which has a memory cell with a stacked capacitor cell" (column 2 lines 8-16) or Fisher et al's teaching of "This invention concerns stacked capacitor cell constructions" (column 1 lines 23-26).

Therefore, Claim 53 is patentable over Turner, Kurosawa et al., and Fisher et al.

CONCLUSION

For the reasons stated above, the Appellant respectfully contends that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

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CLAIMS APPENDIX

49. An integrated circuit comprising:

a first insulating layer disposed between a substrate and a first metal layer;

a trench defined by a recess in the first insulating layer, the trench not extending below a top surface of the substrate;

a first contact pillar extending substantially from the top surface of the substrate to a bottom surface of the first metal layer within the trench; and

a capacitor formed in the trench overlying the first contact pillar such that the capacitor is formed at least in part on a side of the first contact pillar, and the first contact pillar is a first plate of the capacitor.

50. The integrated circuit of claim 49, further comprising a second contact pillar extending substantially from the top surface of the substrate to a bottom surface of another portion of the first metal layer, wherein the second contact pillar is substantially the same height as the first contact pillar.

51. The integrated circuit of claim 49, wherein the capacitor comprises a storage element of a memory cell.

52. The integrated circuit of claim 51, wherein a storage node of the storage element comprises the first contact pillar.

53. The integrated circuit of claim 52, wherein the storage node further comprises a conducting layer lining the trench and the side of the first contact pillar.

54. The integrated circuit of claim 50, wherein the second contact pillar is a bit line contact pillar.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None